REMARKS

Rejections Under 35 USC §102

Claims 52-56 and 70-76 have been rejected under 35 USC §103(a) as being anticipated by Cram in view of Khandros et al.

Claim 77 has been rejected under 35 USC §103(a) as being anticipated by Cram in view of Khandros et al. as applied to claim 60 above, and further in view of Franklin et al.

The rejections under 35 USC §103 are traversed for the reasons to follow. However, the claims have been amended to more clearly define features which patentably distinguish the invention from the prior art. A reading of the claims on the drawings and specification is as follows.

52. A semiconductor component **(Figure 4)** comprising:

a substrate **(10-Figure 4)** comprising a plurality of semiconductor components **(12-Figure 4)** including a plurality of patterns of component contacts **(28-Figure 4)**; and

a plurality of conductors **(22-Figure 2F)** on the components in electrical communication with the component contacts configured to redistribute the patterns of the component contacts into selected patterns **(page 5, lines 11-13)** and to either repair, reconfigure, or electrically isolate selected components **(page 5, lines 13-16)**; and

a plurality of terminal contacts **(64-Figure 7A)** on the components in the selected patterns in electrical communication with the conductors.

53. The component of claim 52 wherein the substrate comprises a semiconductor wafer and the components comprise

semiconductor dice or semiconductor packages on the semiconductor wafer **(page 4, lines 16-19)**.

54. The component of claim 52 wherein the conductors are contained in a metal redistribution layer **(page 4, lines 31-32)**.

55. The component of claim 52 wherein the conductors are configured to electrically connect multiple components in a cluster that excludes at least one defective component **(page 5, lines 16-19)**.

56. A semiconductor component **(Figure 4)** comprising:

a substrate **(10-Figure 4)** comprising a plurality of tested components **(12-Figure 4)** comprising a plurality of component contacts **(28-Figure 4)** in a plurality of patterns;

the components including a plurality of good components and a defective component **(12D-Figure 4)**;

a plurality of conductors **(22-Figure 2F)** configured to redistribute the patterns of the component contacts into selected patterns **(page 5, lines 11-13)**, to provide electrical paths for the component contacts on the good components, and to electrically isolate the component contacts on the defective component **(page 5, lines 16-19)**; and

a plurality of terminal contacts **(64-Figure 7B)** on the good components in the selected patterns in electrical communication with the conductors.

57. The component of claim 56 wherein the conductors are contained in a metal redistribution layer **(page 4, lines 31-32)**.

58. The component of claim 56 wherein the conductors are configured to electrically connect a plurality of good components in a cluster **(page 5, lines 16-19)**.

59. The component of claim 56 wherein the substrate comprises a semiconductor wafer, and the components comprise semiconductor dice or semiconductor packages **(page 4, lines 16-19)**.

60. A semiconductor component **(52-Figure 7-7B)** comprising:

a semiconductor die **(54-Figure 7B)** comprising a plurality of integrated circuits **(56-Figure 7B)** and a pattern of component contacts **(58-Figure 7B)** in electrical communication with the integrated circuits;

a plurality of conductors **(22P-Figure 7B)** on the die in electrical communication with the component contacts configured to redistribute the pattern of the component contacts into a selected pattern **(page 5, lines 11-13)**; and

a plurality of terminal contacts **(64-Figure 7B)** on the die in the selected pattern in electrical communication with the conductors;

at least some of the conductors configured to electrically isolate selected component contacts **(page 14, lines 6-9)**.

61. The component of claim 60 wherein the terminal contacts comprise balls or bumps in a grid array **(page 5, line 13)**.

62. The component of claim 60 wherein the conductors are contained in a metal redistribution layer **(page 4, lines 31-32)**.

63. A test board **(48-Figure 6)** for testing semiconductor components **(12-Figure 6)** on a substrate **(10-Figure 6)** including a plurality of good components and at least one defective component **(12D-Figure 6)**, each component having a plurality of component contacts **(28-Figure 6)**, the test board **(48-Figure 6)** comprising:

a plurality of first test sites **(50-Figure 6)** on the test board comprising a plurality of contacts **(51-Figure 6)** configured to electrically engage the component contacts on the good components on the substrate **(page 15, line 31 to page 16, line 6)**; and

a plurality of second test sites **(50D-Figure 6)** on the test board configured to electrically isolate the defective component **(page 16, lines 7-9)**.

64. The test board of claim 63 wherein the test board includes a patterned metal layer containing a plurality of conductors in electrical communication with the first test sites **(page 16, lines 9-13)**.

65. The test board of claim 63 wherein the test board is configured to perform a burn-in test and the second test sites are configured to electrically isolate the defective component during the burn-in test **(page 15, line 34)**.

66. The test board of claim 63 wherein the substrate comprises a semiconductor wafer, and the components comprise dice or packages **(page 4, lines 16-19)**.

70. A semiconductor component **(52-Figures 7-7B)** comprising:

a semiconductor die **(54-Figure 7B)** comprising a plurality of contacts **(58-Figure 7B)** in a first pattern and a plurality of integrated circuits **(56-Figure 7B)** in electrical communication with the contacts;

a plurality of terminal contacts **(64-Figure 7B)** on the die in a second pattern; and

a metal redistribution layer **(page 4, lines 31-32)** on the die containing a plurality of conductors **(22P-Figure 7B)** configured to redistribute the first pattern of the contacts to the second pattern of the terminal contacts **(page 5, lines 11-13)**, and to either repair, reconfigure, or electrically isolate selected integrated circuits **(page 5, lines 13-16)**.

71. The component of claim 60 wherein the terminal contacts comprise balls or bumps and the second pattern comprises a grid array **(page 5, line 13)**.

72. The component of claim 60 wherein the contacts comprise bond pads **(page 16, line 21)**.

73. The component of claim 60 wherein the conductors fan out from the first pattern to the second pattern **(page 5, lines 11-13)**.

74. The component of claim 60 wherein the component is contained on a substrate **(10-Figure 4)**.

75. The component of claim 60 further comprising a protective layer **(66-Figur 7B)** on the conductors having a plurality of openings **(68-Figur 7B)** for the terminal contacts.

76. The component of claim 60 wherein the component comprises a semiconductor package **(page 16, line 14)**.

77. The component of claim 60 wherein the conductors are configured to repair at least one defective integrated circuit **(page 18, lines 5-7)**.

Argument

The rejections under 35 USC §103 are traversed as the cited combination of Cram and Khandros et al. does not teach or suggest all of the elements of the amended independent claims. Specifically, amended independent claim 52 includes the recitation that the conductors are "configured to redistribute the patterns of the component contacts into selected patterns". Amended independent claims 56, 60 and 70 include similar recitations.

The primary reference to Cram discloses a method for testing semiconductor components in which a semiconductor wafer 10 is provided with a plurality of dice 12. The wafer 10 is also provided with resilient contact structures 14 on each of the dice 12 (column 2, lines 62-64). The wafer 10 is initially tested to identify good dice and non functional dice (column 2, lines 64-66). The resilient contact structures 14 on the defective dice 12 are then deformed to electrically isolate the non functional dice 12 during burn-in testing (column 3, lines 5-9).

Khandros et al. was cited as teaching terminal contacts (840-Figure 8G) on conductors (854-Figure 8G).

In Cram the resilient contact structures 14 (Figure 2A) are attached to the bond pads 16 (Figure 2C) of the dice 12 (column 1, lines 63-66). The resilient contact structures 14 thus have the same pattern as the bond pads 16 on the dice 12. In addition, any terminal contacts on the resilient contact structures 14 would also have the same pattern as the bond pads on the dice 12.

In citing Cram, the Office Action states at page 6, paragraph 3, that the conductors (resilient contact structures 14) comprise "a metal ... redistribution layer (16)". However, the resilient contact structures 14 in Cram do not function to redistribute the bond pads 16 into

a different pattern, such as a grid array, for terminal contacts.

In the presently claimed component the conductors 22 redistribute the pattern of the component contacts 58 to that of the terminal contacts 64. This permits the component contacts 58 to be arranged in a standardized pattern, and the terminal contacts 64 to be arranged in a dense area array, such as a ball grid array. In addition, the conductors 22 can perform multiple electrical functions such as repairing, reconfiguring and isolating integrated circuits. Although Cram teaches electrical isolation for testing, there is no teaching of repairing or reconfiguring of integrated circuits.

With respect to Franklin et al., this reference teaches "a method for repairing interconnections" (abstract) using "metal line repair straps" (column 3, lines 50-53). However, the combination of Cram, Khandros et al. and Franklin et al. still does not teach the feature of redistribution conductors configured to repair defective integrated circuits.

Amended independent claim 63 is directed to a test board 48 (Figure 6). The test board is customized with test sites 50 and 50D (Figure 6) which match the location of the components 12 and the defective components 12D (Figure 6) on a substrate 10. Neither Cram or Khandros et al. even remotely suggest a test board having customized test sites.

With respect to the "laser patterned" feature of the present component, all of the "laser patterned" recitations have been removed from the amended claims.

Conclusion

In view of the amendments and arguments the rejections are submitted to have been overcome, and the claims should be in a condition for allowance. Favorable consideration and allowance of claims 52-66 and 70-77 is respectfully requested. Should any issues arise that will advance this case to allowance, the Examiner is asked to contact the undersigned by telephone.

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